Abstract of the Disclosure

A multi-port memory device includes a plurality of banks arranged at an upper and a lower portion of a core area as many as a fixed number in a row direction, a multiplicity of ports located at edges of the upper and the lower portions of the core area, wherein respective ports perform independent communication with respective different target devices, a first global data bus, located in a row direction between the ports and the banks arranged at the upper portion of the core area, for performing the parallel data transmission, a second global data bus, located in a row direction between the ports and the banks arranged at the lower portion of the core area, for performing the parallel data transmission, many local data buses, arranged in a column direction of each bank, for executing data transmission within the banks, and a majority of local data bus connection units, located between two banks adjacent to each other in a column direction, for selectively connecting the local data buses corresponding to the two adjacent banks.